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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,158	04/13/2004	Fu-Liang Yang	TSM03-0929	4551

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EXAMINER	
DOAN, THERESA T	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,158	YANG ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-14,16,17,38 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39* is/are allowed.

6)☒ Claim(s) *1-8,10-14,16,17 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 9, 15 and 18-37 in paper filed on 04/03/06 is acknowledge.

Claim Objections

2. Claim 17 and new claim 39 are objected to because of the following informalities:

In claim 17, line 3, a phrase "...the semiconductor layer ..." should be changed to "...**a** semiconductor layer ...".

In new claim 39, last 2 lines, a phrase "...source and drain regions formed in the second portion ..." should be changed to "...source and drain regions formed in the first portion ..." which refers to "the first portion" 51 of the planar transistor shown in Fig. 5.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 10-11, 13-14, 17 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doris et al. (U.S. Pat. 6,911,383) in view of Joshi et al. (20050017377).

Regarding claims 1 and 13, Doris (Figs. 10-14) discloses an insulator layer 14 (column 4, lines 37-41); a planar transistor 34 formed on a first portion of a semiconductor layer 16, the first portion of the semiconductor layer 16 overlying the insulator layer 14, and the first portion of the semiconductor layer 16 having a first thickness h_2 (Fig. 10, column 6, lines 62-65); and a multiple-gate transistor 32 formed on a second portion of the semiconductor layer 16, the second portion of the semiconductor layer 16 overlying the insulator layer 14, the second portion of the semiconductor layer 16 having a second thickness h_1, and the second thickness h_1 being larger than the first thickness h_2 (Fig. 10, column 6, lines 62-66 and column 7, lines 23-26), wherein the multiple-gate transistor 32 comprises: a vertical semiconductor fin 16 formed from the second portion of the semiconductor layer; a gate dielectric 40 (see Fig. 12) having vertical portions on opposite sidewalls of a channel portion of the semiconductor fin 16; a gate electrode 42 (also see Fig. 12) overlying the gate dielectric 40, wherein the gate electrode 42 has vertical portions on the vertical portions of the gate dielectric 40; and source and drain regions 16 formed in the second portion of the semiconductor layer oppositely adjacent the gate electrode 42.

Doris does not disclose the gate dielectric 40 having a horizontal portion formed on the top surface of the channel portion of the semiconductor fin 16, and the gate electrode 42 having a horizontal portion formed on the horizontal portion of the gate dielectric 40.

However, Joshi (Fig. 8C) teaches a tri-gate transistor 92 comprising a gate dielectric 33 having vertical portions on opposite sidewalls of a channel portion of the

semiconductor fin and a horizontal portion on a top surface of the channel portion of the semiconductor fin, and a gate electrode 97 overlying the gate dielectric 33, wherein the gate electrode 97 has vertical portions on the vertical portions of the gate dielectric 33 and a horizontal portion on the horizontal portion of the gate dielectric 33.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the multiple-gate transistor of Doris by forming the gate dielectric 40 having a horizontal portion formed on the top surface of the semiconductor fin and by forming the gate electrode 42 having a horizontal portion formed on the horizontal portion of the gate dielectric 40 because the forming of such gate dielectric and gate electrode structures would provide a triple gate Fin FET, as taught by Joshi (see paragraph [0046], lines 8-11).

Regarding claim 2, Doris further discloses that the semiconductor layer 16 comprises a material selected from a group consisting of silicon, germanium, silicon germanium, and combinations thereof (column 4, lines 46-49).

Regarding claim 3, Doris (Fig. 10) discloses that the insulator layer 14 comprises silicon oxide (column 4, lines 55-58).

Regarding claim 6, Doris discloses that the planar transistor 34 comprises: a planar channel 34 formed from the first portion of the semiconductor layer 16 (column 6, lines 62-65); a gate dielectric 40 overlying at least a portion of the planar channel 34

(Fig. 11, column 7, lines 54-56); a gate electrode (42,46) overlying the gate dielectric 40 (Figs. 12-13, column 7, lines 57-67 and column 8, lines 1-7); and source and drain regions (not shown) formed in the first portion of the semiconductor layer 16 oppositely adjacent the gate electrode 46 (column 8, lines 45-49).

Regarding claims 7 and 10, Doris (Fig. 10) discloses that the gate dielectric 40 comprises a material selected from a group consisting of silicon oxide and silicon oxynitride (column 7, lines 42-46).

Regarding claims 8 and 11, Doris (Fig. 10) discloses that the gate electrode (42,46) comprises a material selected from a group consisting of a metal, a metallic silicide, polysilicon, and combinations thereof (column 7, lines 63-67).

Regarding claims 4-5 and 14, Doris does not disclose that the first thickness is less than about 400 Å and the second thickness is greater than about 100 Å.

However, Doris's Fig. 10 teaches the thickness of the top semiconductor layer 16 is about 100 to 1000 Å (column 5, lines 6-7) and an optional thinning step may follow the bonding process. The optional thinning step reduces the thickness of the top semiconductor 16 to a layer having a thickness that is more desirable (column 5, lines 2-5). It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.* Therefore, it would have been obvious to one having

ordinary skill in the art at the time of the invention was made to modify the first and second thickness of Doris by forming the first thickness is less than about 400 Å and the second thickness is greater than about 100 Å because the changes in thickness of semiconductor layer for the first thickness and the second thickness can be varied depending upon the size that desired for the semiconductor device such as a planar transistor or a multiple-gate transistor.

Regarding claim 17, as discussed in details above, the combination of Doris (Figs. 10-14) and Joshi (Fig. 8C) substantially reads on the invention as claimed, including the limitations of forming a planar transistor on a first portion of a semiconductor layer and forming a multiple-gate transistor on a second portion of the semiconductor layer, wherein the second portion having a second thickness being greater than the first thickness of the first portion, and wherein the multiple-gate transistor comprises: a gate dielectric having vertical portions and a horizontal portion formed on sidewalls and top surface of the semiconductor fin, and a gate electrode having vertical portions and a horizontal portion formed on the vertical portions and the horizontal portion of the gate dielectric.

Doris does not disclose that the first thickness is less than about 400 Å and the second thickness is greater than about 100 Å.

However, Doris's Fig. 10 teaches the thickness of the top semiconductor layer 16 is about 100 to 1000 Å (column 5, lines 6-7) and an optional thinning step may follow the bonding process. The optional thinning step reduces the thickness of the top

semiconductor 16 to a layer having a thickness that is more desirable (column 5, lines 2-5). It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.* Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the first and second portions of the semiconductor layer having the first and second thickness in a range as claimed because the thicknesses of the first and second portions of the semiconductor layer can be desired (as taught by Doris, column 5, lines 2-5) depending upon the sizes that are desired for the planar transistor and the multiple-gate transistor.

Regarding claim 38, Doris (Fig. 14) also discloses that the gate dielectric 40 of the planar transistor 34 extends entirely on the channel and source/drain regions (not shown in drawing, see column 8, lines 45-47), the gate dielectric 40 comprises a portion on a top surface of the planar channel and portions on the boundary of the channel sidewalls formed between source/drain regions and the channel region.

5. Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doris et al. (U.S. Pat. 6,911,383) and Joshi et al. (US PUB. 20050017377) as applied to claims 1 and 13 above, and further in view of Hieda (US PUB. 2002/0011612).

Neither Doris nor Joshi discloses that corners of the semiconductor layer are rounded at edges of active regions of the planar and multiple-gate transistors.

However, Hieda (Figs. 28 and 66) teaches a semiconductor device having a rounded top corner channel semiconductor layer 15 (paragraph [0187]), as shown in Fig. 28, the influence of the electric field from the gate electrode 16 can be remarkable decreased (see paragraphs [0318] to [0320]). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device of Doris by forming the corners of the semiconductor layer are rounded at edges of active regions of the planar and multiple-gate transistors because such a forming structure of a round of the top corner of the semiconductor layer would decrease the influence of the electric field from the gate electrode and the pressure endurance of the gate insulating can be improve, as taught by Hieda (see paragraphs [0318] to [0320]).

Allowable Subject Matter

6. New claim 39 is allowed.

7. The following is an examiner's statement of reasons for allowance:

The prior art of record fails to disclose all the limitations recited in the new claim 39; including the combination of the limitations forming a planar transistor on a first portion of a semiconductor layer and forming a multiple-gate transistor formed on a second portion of the semiconductor layer, wherein the second portion has a second thickness being larger than the first thickness of the first portion, and wherein the planar transistor comprises: a gate dielectric having vertical portions and a horizontal portion on sidewalls and top surface of the planar channel, and a gate electrode having vertical

portions on the vertical portions of the gate dielectric and a horizontal portion on the horizontal portion of the gate dielectric.

Response to Arguments

8. Regarding claims 1-8, 10-14 and 17, Applicant argues that Doris fails to disclose that the multiple-gate transistor is a triple gate transistor as recited in amended independent claims 1, 13 and 17 because the multiple-gate transistor 32 is a double-gate device comprising two gates on sidewalls of the semiconductor layer 16, and no gate at the top of the semiconductor layer 16.

However, because this is a new issue, the new reference issued to Joshi et al. is applied in the new ground of rejection. Joshi (Fig. 8C) specifically teaches a multiple-gate transistor comprising the gate electrode 97 having vertical portions on the vertical portions of the gate dielectric 33 and a horizontal portion on the horizontal portion of the gate dielectric 33. Therefore, it would have been obvious to modify the double-gate transistor of Doris by forming the gate electrode not only on the vertical portions of the gate dielectric but also on the horizontal portion of the gate dielectric in order to provide a triple gate Fin FET, as taught by Joshi (see paragraph [0046], lines 8-11).

9. Regarding claim 38, Doris (Fig. 14) also discloses that the gate dielectric 40 of the planar transistor 34 extends entirely on the channel and source/drain regions (not shown in drawing, see column 8, lines 45-47), the gate dielectric 40 comprises a portion

on a top surface of the planar channel and portions on the boundary of the channel sidewalls formed between the source/drain regions and the channel region.

10. Regarding new claim 39, new claim 39 is allowed because the prior art of record fails to disclose the planar transistor structure as recited, including the forming of a gate dielectric on the vertical portions of the planar channel and on the top surface of the planar channel, and forming of the gate electrode on the vertical portions of the gate dielectric and on the horizontal portion of the gate dielectric.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan
June 9, 2006.

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06/01/06

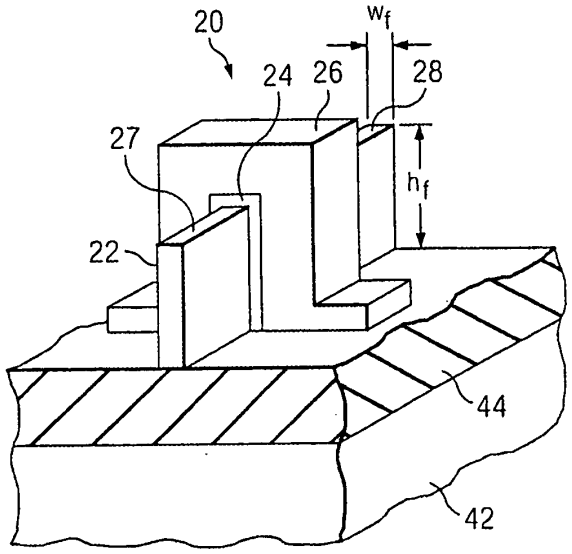

FIG. 1 (PRIOR ART)

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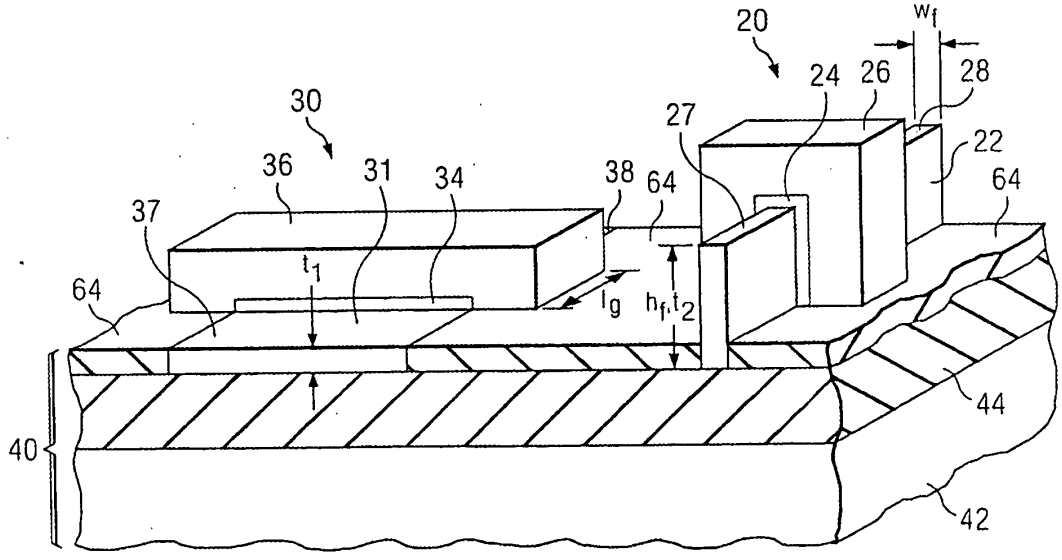

FIG. 2